CLAIM AMENDMENTS

IN THE CLAIMS

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1. (Currently Amended) A pulse width modulator for a processor having pulse width modulation (PWM) outputs that are configured to operate based on configuration bits when pulse width modulation outputs are not enabled, comprising:

output control logic;

configuration bits for selectively configuring the output control logic; and

an output transistor pair having upper and lower transistors that are respectively coupled to opposing output voltage levels;

the configuration bits causing the output control logic to configure the output pair to operate in any one of a tri-state, active high or active low mode when the is not enabled for PWM data output.

2. (Original) The pulse width modulator according to claim 1, wherein the configuration bits include a tri state control bit that configures the output pair to operate in one of a tri-state or an active mode.

3. (Original) The pulse width modulator according to claim 2, wherein the configuration bits include a high device set bit that configures the output pair to operate in one of an active high or an active low mode when the tri-state control bit configures the output pair to operate in an active mode.

4. (Original) The pulse width modulator according to claim 3, wherein the output pair outputs a signal to an external device in an high arrangement.

5. (Currently Amended) The pulse width modulator according to claim 2, wherein the configuration bits include a ~~high~~ low device set bit that configures the output pair to operate in one of an active high or an active low mode when the tri-state control bit configures the output pair to operate in an active mode.

6. (Original) The pulse width modulator according to claim 5, wherein the output pair outputs a signal to an external device in an low arrangement.

7. (New) The pulse width modulator according to claim 1, further comprising a memory to store said plurality of configuration bits.

8. (New) A processor comprising:

a processing core;

memory operably associated with said processing core;

a plurality of pulse width modulation (PWM) outputs;

output control logic coupled to each of the plurality of PWM outputs, said output control logic comprising at least one input to receive a plurality of configuration bits from said memory; and wherein

the output control logic, in response to receiving the configuration bits, configures respective PWM outputs to operate in a tri-state, active high or active low mode if the respective PWM outputs are not enabled for PWM data output.

9. (New) The processor according to claim 8, wherein the configuration bits include a tri state control bit to configure the respective PWM output to operate in one of a tri-state or an active mode.

10. (New) The processor according to claim 9, wherein the configuration bits include a high device set bit to configure the respective PWM outputs to operate in one of an active high or an active low mode when the tri-state control bit configures the respective PWM outputs to operate in an active mode.

11. (New) The processor according to claim 10, wherein the respective PWM outputs provide a signal to an external device in an high arrangement.

12. (New) The processor according to claim 9, wherein the configuration bits include a low device set bit to configure the respective PWM outputs to operate in one of an active high or an active low mode when the tri-state control bit configures the respective PWM outputs to operate in an active mode.

13. (New) The processor according to claim 12, wherein the respective PWM outputs provides respective signal to an external device in an low arrangement.

14. (New) A method comprising:

receiving a plurality of configuration bits at an output controller of a pulse width modulator, the output controller being coupled to a plurality of pulse width modulated (PWM) outputs; and

if respective PWM outputs are not enabled for PWM data output, configuring individual ones of the plurality of PWM outputs to operate in a tri-state, active high or active low mode in response to receiving the plurality of configuration bits.

15. (New) The method according to claim 14, wherein each of the plurality of PWM outputs comprises an output transistor pair having upper and lower transistors, the upper and lower transistor coupled, respectively, to opposing output voltage levels.

16. (New) The method according to claim 14, further comprising configuring the respective PWM outputs to operate in one of a tri-state or an active mode based, at least in part, on a tri-state control bit.

17. (New) The method according to claim 16, further comprising configuring the respective PWM outputs to operate in one of an active high or an active low mode in response to a high device set bit, if the respective PWM outputs are operating in an active mode.

18. (New) The method according to claim 17, further comprising providing an output signal from the respective PWM outputs to an external device in an high arrangement.

19. (New) The method according to claim 16, further comprising configuring the respective PWM outputs to operate in one of an active high or an active low mode in response to a low device set bit, if the respective PWM outputs are operating in an active mode.

20. (New) The method according to claim 19, further comprising providing an output signal from the respective PWM outputs to an external device in an low arrangement.